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INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 : H01L 29/768, 29/207, 21/22, 21/339

A1

(11) International Publication Number: WO 98/11608

(43) International Publication Date: 19 March 1998 (19.03.98)

(21) International Application Number: PCT/IB97/00890

(22) International Filing Date: 17 July 1997 (17.07.97)

(30) Priority Data:
96202523.5 10 September 1996 (10.09.96) EP
(34) Countries for which the regional or international application was filed: NL et al.

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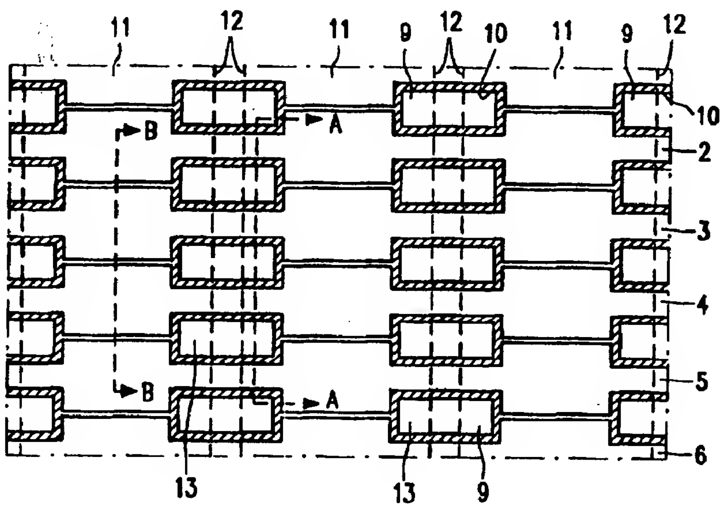
(81) Designated States: JP, KR, European patent (AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

Published
With international search report.
Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.

(54) Title: CHARGE COUPLED DEVICE, AND METHOD OF MANUFACTURING SUCH A DEVICE



(57) Abstract

It is known in charge coupled devices to use a dual layer of silicon oxide and silicon nitride as the gate dielectric. Since silicon nitride is practically impermeable to hydrogen, the nitride layer is usually provided with openings through which hydrogen can penetrate up to the surface of the silicon body during the annealing step carried out for passivating the surface. The openings in the nitride layer are provided by a known method, with gates in a first poly layer serving as a mask, in that the nitride is removed from between these gates and an oxidation step is subsequently carried out. According to the invention, the openings in the nitride layer are formed by means of a separate mask (20), such that the edges of the openings (9) in the nitride layer (8) lie at some distance from the edges of the gates. It was found that the dark current can be substantially reduced by this method, and that in addition quantities such as the fixed pattern noise and the number of white spots can be advantageously reduced.

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Charge coupled device, and method of manufacturing such a device.

The invention relates to a charge coupled device with a semiconductor body which is provided at a surface with a system of silicon electrodes to which voltages can be applied for controlling the storage and transport of electric charges in the semiconductor body, which electrodes are separated from the surface at least locally by a dielectric layer comprising a dual layer of silicon oxide and silicon nitride, the latter being locally provided with openings. The invention also relates to a method of manufacturing such a charge coupled device.

A charge coupled device and a method of the kind as described above are known inter alia from US Patent 4,077,112. A device is described therein where the electrodes are formed in two or more layers of polycrystalline silicon (referred to as poly hereinafter). In a first step, the (active portion of the) surface of the semiconductor body is covered with gate oxide on which subsequently a layer of silicon nitride is deposited. The first poly layer is provided thereon, and a number of electrodes are formed from the poly layer by known photolithographic means. Said electrodes are covered with a layer of silicon oxide by thermal oxidation, this layer forming an electrical insulation layer against any subsequent poly layer. During the oxidation step, the portion of the surface not covered with poly is masked against oxidation by the silicon nitride layer, whereby it is prevented that the gate oxide becomes thicker locally than is desired. After the oxidation, openings are formed in the silicon nitride layer through etching in a self-aligned manner, the poly electrodes formed with the oxide layer present thereon acting as an etching mask during this. As is described in the Patent, these openings in the nitride layer are necessary for efficiently passivating the surface in a later stage through annealing in hydrogen. This is because the density of silicon nitride is usually so great that, without openings in the silicon nitride layer, the hydrogen would be incapable of reaching the surface of the semiconductor body everywhere. A light oxidation step is subsequently carried out which renders the thickness of the uncovered gate oxide somewhat greater. Then a second conductive layer is deposited from which electrodes are formed next to the electrodes already present and electrically

insulated therefrom by the oxide layer on the electrodes which were provided first.

As was noted above, the surface of the semiconductor body can be effectively passivated through heating in an environment containing hydrogen, during which hydrogen can spread through the openings in the nitride over the surface through diffusion. This step considerably reduces the concentration of surface states, and thus the leakage current. A reduction in the leakage current is of particular, though not exclusive importance in charge coupled imaging devices because local leakage currents may give rise to a greater spread in the dark current, and thus to an uneven picture on a display device.

The present invention has for its object inter alia to reduce the leakage current still further.

According to the invention, a charge coupled device of the kind described in the opening paragraph is for this purpose characterized in that the openings in the silicon nitride layer are bounded by edges which, seen transverse to the surface, lie at a distance from the edges of adjoining electrodes. The invention is based inter alia on the recognition that an oxide with a LOCOS-type structure is formed in the openings in the silicon nitride layer in the known device. The transition from this LOCOS oxide to the original, thinner gate oxide via a so-called bird's beak, the location of which is defined by the edges of the openings in the silicon nitride layer, coincides with the edges of the poly electrodes which are present. The invention is furthermore based on the recognition that the presence of the poly electrodes above the bird's beak may induce additional mechanical stresses in the subjacent active region, which stresses cause an increase in the leakage current or, in the case of an imaging device, the dark current. In a charge coupled device according to the invention, the edges of the poly electrodes do not coincide with the edges of the openings in the nitride layer, so that major leakage currents are avoided.

The invention offers particular advantages when the surface area of the charge coupled device is very large, because in such cases the openings in the silicon nitride layer are important for the lateral spread of the hydrogen over the entire device. A major embodiment according to the invention is characterized in that the device comprises a number of parallel charge transport channels which form a matrix in which charge packets can be stored in a bidimensional pattern and can be transported in parallel to read-out means. The device may be, for example, a memory of the SPS type here where (digital) information is put in in series, is transported in parallel through the matrix, and is read out in series

again.

An embodiment for which a low and uniform leakage current is particularly important, because non-uniformities in the leakage current will become visible again upon the display of the image, is characterized in that the device forms a charge coupled imaging device.

A preferred embodiment of a charge coupled imaging device according to the invention is characterized in that the system of electrodes forms openings, referred to as windows, which transmit electromagnetic radiation, within which the surface is not covered by material of the electrodes, and which are situated between mutually adjoining charge transport channels. Since the electromagnetic radiation can reach the photosensitive portion of the device through said windows without passing through the poly material of the electrodes, the sensitivity of the imaging device will be high. A further embodiment is characterized in that the openings in the silicon nitride layer are formed at the areas of said windows, the edges of the openings lying at a distance from the edges of the windows. Preferably, the distance between the edges of the openings in the silicon nitride layer and the edges of the windows is chosen to be equal to or greater than 1.0 μm so as to minimize the influence of the edges of the electrodes on the bird's beak and thus to minimize the leakage current. Since there will always be a certain increase in the leakage current at the areas of the openings in the silicon nitride layer, it is advantageous to drain off this leakage current as much as possible through channel bounding zones. Accordingly, a further embodiment is characterized in that mutually adjoining charge transport channels in the semiconductor body are separated from one another substantially only by a channel bounding region, the openings in the silicon nitride layer being situated above the channel bounding regions.

A further embodiment of a charge coupled imaging device according to the invention, in which the openings in the silicon nitride layer can be provided independently of the positions of radiation-transmitting windows in poly layers, is characterized in that at least a number of the openings in the silicon nitride layer is provided between the surface of the semiconductor body and electrodes which extend over the openings. If the electrodes in this embodiment are provided with radiation-transmitting windows, the silicon nitride can also be removed at the areas of these windows through the use of a mask. A preferred embodiment, which has the advantage that no oxidation is necessary at the areas of these windows, is characterized in that the surface is covered by portions of the silicon nitride layer at the areas of the radiation-transmitting windows.

Various designs are possible when the electrodes are manufactured from

two or more poly layers. Thus the openings may be formed in the silicon nitride layer before the deposition of the first poly layer or after the deposition of the first poly layer and before deposition of a second or third poly layer. An important embodiment of the invention is characterized in that the electrodes are formed from two or more layers of silicon, electrodes formed from a first silicon layer being separated from the surface by a first layer of silicon nitride provided with said openings, and electrodes formed from a second layer of silicon being insulated from the electrodes of the first layer of silicon by a second silicon nitride layer which is also provided with openings.

A method according to the invention for manufacturing a device as described above is characterized in that the openings in the silicon nitride layer are defined by means of an etching mask which was formed by way of photolithography and is provided with openings through which the silicon nitride layer is subjected to an etching treatment.

These and other aspects of the invention will be explained in detail with reference to a few embodiments. In the drawing:

Fig. 1 is a plan view of a charge coupled device according to the invention;

Figs. 2 to 5 show cross-sections through this device taken on the lines A-A and B-B during various stages in the manufacture of the device;

Fig. 6 is a plan view of a second embodiment of a device according to the invention;

Fig. 7 is a plan view of a third embodiment of a charge coupled device according to the invention;

Fig. 8 is a cross-section of this device taken on the line VIII-VIII in Fig. 7;

Fig. 9 is a plan view of a further embodiment of a charge coupled device according to the invention;

Fig. 10 is a plan view of yet another embodiment of a charge coupled device according to the invention; and

Fig. 11 is a plan view of a yet further embodiment of a charge coupled device according to the invention.

Fig. 1 is a plan view of part of a charge coupled device according to the invention. Figs. 5a and 5b show cross-sections through this device taken on the lines A-A and B-B, respectively. The device comprises a semiconductor body 1 of silicon which is provided at its surface with a system of electrodes 2-6 manufactured from doped silicon which usually has the polycrystalline form, and is accordingly referred to as poly hereinafter. As is known, clock voltages can be applied to the electrodes 2-6 by voltage means not shown in the drawing, such that information in the form of packets of electric charge can be generated and transported to read-out means (also not shown) in a controlled manner. The electrodes are insulated from the silicon of the semiconductor body by means of a dielectric layer which comprises a dual layer at least locally, formed by a layer 7 of silicon oxide and a layer 8 of silicon nitride. As will become apparent below, the nitride prevents oxidation of the surface of the semiconductor body 1 during oxidation of the poly electrodes. The silicon nitride is locally provided with openings 9 because hydrogen is practically incapable of diffusing through the silicon nitride. During production, hydrogen can diffuse through these openings along the surface in a heating step and reduce the number of surface states, and thus the leakage current in the device, for example by binding itself to dangling bonds of the silicon crystal. Reference may be made to the cited Patent US-A 4,077,112 in this connection.

According to the invention, the openings are provided such that the edges 10 of the openings 9, seen transverse to the surface of the semiconductor body, lie at a distance from the edges of adjoining electrodes 2-6. Since the openings in the nitride layer 8 serve to enable hydrogen diffusion, the invention is particularly, though not exclusively important for devices having a large surface area with a number of charge transport channels 11 (three of which are shown in Fig. 1, but the actual number is usually much higher), which form a matrix in which charge packets can be stored in a bidimensional pattern and can be transported in parallel to an output which is not shown in the drawing. Such a matrix may be a memory, for example of the SPS type. In the present embodiment, the matrix forms part of a charge coupled imaging device. The device may be of the interline type, in which the photosensitive elements are formed by photodiodes arranged in rows and columns, while charge transport channels 11 are formed between the columns for the charge transport. In the present embodiment, the photosensitive elements are formed by the charge coupled device itself, and the generation of charge caused by the absorption of light takes place in the charge transport channels 11 which are separated from one another exclusively by the channel bounding zones 12. To increase the sensitivity, the system of electrodes 2-6 is

provided with radiation-transmitting windows 13 within which the surface of the semiconductor body is not covered with poly, so that light can reach the semiconductor body 1 directly at the areas of these windows without being partly absorbed by poly. The openings 9 in the silicon nitride layer 8 are situated concentrically in the windows 13 such that the edges of the openings in the silicon nitride lie at some distance away from the edges of the radiation-transmitting windows 13. In Fig. 1, the portions of the silicon nitride layer which project beyond the poly are marked with crosses for clarity. The effect of this measure is shown in Fig. 5a. After the annealing step in hydrogen, an oxidation step is carried out whereby LOCOS-type thickenings are formed in the oxide layer 7 at the areas of the openings 9 in the nitride layer. It was found in practice that the leakage current in the device can be reduced considerably further through a lateral separation of the electrodes 2-6 from the LOCOS 14, compared with a known device in which the openings 9 in the nitride layer, and thus also the LOCOS 14, are aligned with the electrodes. A possible explanation could be that stresses are induced in the silicon crystal lattice, generating additional leakage currents, especially at the edge of the LOCOS (bird's beak). If the openings in the nitride layer coincide with the edges of the electrodes, the bird's beak of the LOCOS will also coincide with the edges of the electrodes, which could give rise to additional mechanical stresses in the lattice and thus to additional leakage currents. Making the openings in the nitride layer smaller than the windows 13 in the electrodes, according to the present invention, achieves that the bird's beak does not lie below the poly, so that mechanical stresses in the crystal lattice and thus the generation of leakage currents in the charge coupled device are reduced. The distance between the nitride edges 10 and the edges of the window 13 is at least approximately 1 μm for obtaining a satisfactory suppression of the leakage current.

A few steps in the manufacture of the device will now be described with reference to Figs. 2-5, each Figure comprising a part a which is a cross-section taken on the line A-A and a part b which is a cross-section taken on the line B-B in Fig. 1. The device which is described here by way of example is of a type known per se, i.e. an N-channel buried channel device with vertical antiblooming. The device is for this purpose provided with a semiconductor body 1 of known construction, with an N-type silicon substrate 15 which forms a draining-off region for excess electrons. The substrate 15 is provided at its surface with one (or several) P-type well(s) 16 in which the N-type CCD channels 11 are formed, mutually separated by the P-type channel bounding zone 12. The depth and doping concentrations of the various N-type and P-type doped regions are chosen such that a

potential barrier is formed in the P-type zone 16 below the channel 11 (cf., for example, Fig. 2a), which barrier has a level at which, once a certain pixel has been completely filled upon local overexposure, excess electrons will flow over this barrier to the substrate so as to be drained off there without filling adjoining pixels. The surface of the semiconductor body 1 is covered with a dielectric layer which is a dual layer here comprising a layer 7 of silicon oxide of a thickness of, for example, 62 nm, and a layer 8 of silicon nitride of a thickness of approximately 75 nm. A first poly layer (polycrystalline silicon) is deposited thereon, which is doped and from which the electrodes 2, 4, 6, etc. are formed by photolithographic means. These electrodes are comparatively narrow at the areas of the windows 13 to be formed (Fig. 2a) and comparatively wide between these windows (Fig. 2b). The electrodes 2, 4, 6 are subsequently subjected to an oxidation step whereby the upper surfaces and the lateral edges of the electrodes are covered with a layer 17 of silicon oxide to a thickness of approximately 200 nm. During the oxidation step, the thickness of the oxide layer 7 does not or at least substantially not increase owing to the presence of the nitride layer 8. Then a layer 18 of silicon nitride, for example 40 nm thick, is provided over the entire assembly. This nitride layer forms a coherent layer with the nitride layer 8 already present between the electrodes 2, 4, 6, etc., but on the electrodes 2, 4, 6 etc. the nitride layer 18 forms a separate layer. Fig. 2 shows the device in this stage.

In a next stage, a second, doped poly layer is provided, and the electrodes 3, 5, etc. are provided in this poly layer between the electrodes 2, 4, etc. alreay present by photolithographic means (Fig. 3). As is shown in the Figure, the electrodes are narrow at the areas of the cross-section a-a, so that light-transmitting windows entirely free from poly are formed here; the electrodes are wide at the areas of the cross-section b-b, and thus cover the entire space. After the definition of the poly electrodes 3, 5, etc., another oxidation step is carried out whereby the electrodes 3, 5 are covered with an oxide layer 19 with a thickness of approximately 200 nm. This stage of the process is shown in Fig. 3. The surface of the semiconductor body 1 and of the electrodes 2, 4, 6 is masked against oxidation by the combined nitride layers 8, 18 during this oxidation.

In a next stage shown in Fig. 4, an etching mask 20 is provided in the form of a suitable photoresist layer. The mask has openings 21 which define the openings 9 to be formed in the nitride layer. The mask 20 overlaps the electrodes 2-6 on either side, as is visible in Fig. 4a, so that the openings 21 will not coincide with the edges of the electrodes. The nitride in poly I may be retained over the electrodes 2, 4, etc. above the CCD channels, if so desired. Preferably, however, this nitride is removed as much as

possible for improving the sensitivity. This is why the mask 20 in the present example is provided with openings 22 (Fig. 4b) above the electrodes 2, 4, 6 and extending over substantially the entire width of the channels 11, while extending next to the windows 13 at most over a distance which is a function of alignment tolerances. Then the nitride layer 8, 18 is provided with the openings 9 within the light-transmitting windows 13, see Fig. 5, by plasma etching in, for example, a mixture of Cl_2 and HBr. At the same time, openings 23 are also formed in the nitride layer 18 on the electrodes 2, 4, 6. The photoresist of the mask 20 may be removed by a usual method after etching of the nitride.

The device is once more subjected to an oxidation treatment after this, inter alia for adjusting the dielectric thickness of the layer again. Certain defects introduced through etching can also be removed by means of such an oxidation step. This oxidation causes the oxide layer 7 in the openings 9 in the nitride layer 8, 18 to grow, whereby the LOCOS-type thickenings 14 are formed at the areas of these openings, see Fig. 5a. The oxide layer 19 on the electrodes 2, 4, 6 at the areas of the openings 23 in the nitride layer 18 also becomes thicker during this, so that here the LOCOS-type thickenings 24 are formed, see Fig. 5b. The device may subsequently be subjected to the usual further process steps, in particular a heating step in an environment containing hydrogen at a temperature of approximately 450 °C for passivating the surface. The hydrogen molecules can diffuse through the openings 9 and 23 in the nitride layer towards and along the surface during this and attach themselves to the dangling bonds of the silicon crystal there.

It was found in measurements that the placement of the openings 9 at a distance from the electrodes can provide a reduction in the dark current by a factor of 4 to 10. In addition, a considerable reduction was obtained in the FPN (fixed pattern noise), i.e. by a factor of 2 to 4, and in the number of defects in the form of white dots.

It is noted that the device described here may form part of an imaging device of the frame transfer type. Such a device has, as is known, a memory matrix besides the photosensitive matrix described above. When a picture has been absorbed during an integration period and converted into a bidimensional pattern of charge packets, this pattern can be quickly transported into the memory matrix. The information can be read out line by line in the memory section while a new picture is captured in the imaging section. The memory matrix may advantageously be provided with openings in the nitride layer as well, in the same manner as the imaging section. If so desired, however, these openings may be omitted in the memory section. This may result in a higher leakage current in the memory section. This higher leakage current (as long as it does not become too high, of course) need

not necessarily be a major disadvantage because this component substantially has the same value for the pixels within a column, because the pixels are continuously displaced, which renders it possible to compensate for this component by electronic means. Such a compensation is less easy for the leakage current in the imaging section because the leakage current is a different one for the different pixels in a column in principle.

Fig. 6 is a plan view of a modification of the device of Fig. 1. The openings 9 in the nitride layer in this modification are dimensioned relative to the channel boundary zones 12 such that the openings 9 lie entirely above the channel bounding zones 12. The region within the semiconductor body where lattice stresses may be induced owing to the LOCOS edge is entirely or at least substantially entirely limited to the zones 12 in this embodiment. Since these zones are not in the depleted state during operation of the device, these lattice stresses do not or at least substantially not lead to an increase in the leakage current.

Figs. 7 and 8 show a further embodiment, in plan view and in cross-section, respectively, which may be used to advantage when the light-transmitting windows 13 in the system of electrodes are so small that no openings in the nitride layer can be provided therein. In that case the openings 9 may be formed, for example, below the electrodes 2, 4, etc. in the first poly layer. These openings are provided before the first poly layer is deposited, for example again at the areas of the P-type channel bounding zones 12. The dimensions and the localization of the openings 9 relative to the poly electrodes are such again that the edges of the openings 9 are at a distance of 1 μm or more from the poly edges. Then a light oxidation step is performed by which the oxide of the layer 7 is made somewhat thicker locally. Poly I is subsequently provided, and the poly electrodes 2, 4, etc. are formed therefrom in a usual manner. These gates are provided with the oxide layer 17 through thermal oxidation. Then the poly II is deposited, from which the gates 3, 5, etc. are formed. Hydrogen can reach the surface of the semiconductor body through the poly gates and the openings 9 in the nitride layer during annealing in this embodiment. The light-transmitting windows 13 in this embodiment may remain covered with nitride, which has the advantage that it is prevented that impurities reach the surface through these windows.

Fig. 9 shows a modification of the embodiment of Figs. 7 and 8 in plan view, where a second nitride layer is deposited, similar to the nitride layer 18 in the first embodiment, after the poly electrodes 2, 4 have been defined in the first poly layer. In this case openings 23 are also provided in the second nitride layer above the electrodes 2, 4 besides the openings 9 in the first nitride layer below the first poly layer. During the

annealing step, hydrogen can reach the surface of the semiconductor body through these openings 23, and the subjacent poly and the openings 9 in the first nitride layer. The opening 23 shown in Fig. 9 is defined in a usual manner by means of a mask. In a modification of this method, a maskless etching step may alternatively be carried out for obtaining the openings 23 because there are two nitride layers present in the windows 13. Etching is continued until the second nitride layer has been completely removed in those locations where it was not covered with poly. No nitride is then present any more above the poly I, whereas the first nitride layer is still present (wholly or in part) in the windows 13.

The channel bounding regions 12 and the light-transmitting windows 13 may be so small that it is not very well possible with the present photolithographic techniques to provide the openings 9 in the nitride layer below the first poly layer above the channel bounding regions 12 and/or in the windows 13. In that case the openings 9 in the (first) nitride layer may alternatively be provided above the active region, i.e. above the charge transport channels 11, as is depicted in Fig. 10. This drawing only shows openings 9 situated below the first poly layer. If a second nitride layer covering the electrodes 2, 4 etc. is provided after the definition of the electrodes in the first poly layer and before the deposition of the second poly layer, openings may be provided in this nitride layer above the electrodes 2, 4, similar to the openings 23 in the preceding embodiment.

Fig. 11 is a plan view of an embodiment in which the poly electrodes 2, 3, 4 cover the entire surface area and are not provided with light-transmitting windows 13 as in the preceding examples. The openings 9 in such an embodiment may be provided above the channels 11 as indicated in Fig. 11, but they may alternatively be formed above the channel bounding zones 12. If a second nitride layer 18 is used, this layer may again be removed from above the electrodes 2, 4 in the first poly layer by one of the methods described with reference to Fig. 9.

It will be obvious that the invention is not limited to the embodiments described here, but that many more variations are possible to those skilled in the art within the scope of the invention. Thus the invention may also be applied to embodiments having more than two poly layers.

The invention may also be used to advantage in other types of charge coupled devices besides the ones described here, for example, in sensors of the interline type.

Claims:

1. A charge coupled device with a semiconductor body which is provided at a surface with a system of silicon electrodes to which voltages can be applied for controlling the storage and transport of electric charges in the semiconductor body, which electrodes are separated from the surface at least locally by a dielectric layer comprising a dual layer of silicon oxide and silicon nitride, the latter being locally provided with openings, characterized in that the openings in the silicon nitride layer are bounded by edges which, seen transverse to the surface, lie at a distance from the edges of adjoining electrodes.

2. A charge coupled device as claimed in Claim 1, characterized in that the device comprises a number of parallel charge transport channels which form a matrix in which charge packets can be stored in a bidimensional pattern and can be transported in parallel to read-out means.

3. A charge coupled device as claimed in Claim 2, characterized in that the device forms a charge coupled imaging device.

4. A charge coupled device as claimed in Claim 3, characterized in that the system of electrodes forms openings, referred to as windows, which transmit electromagnetic radiation, within which the surface is not covered by material of the electrodes, and which are situated between mutually adjoining charge transport channels.

5. A charge coupled device as claimed in Claim 4, characterized in that the openings in the silicon nitride layer are formed at the areas of said windows, the edges of the openings lying at a distance from the edges of the windows.

6. A charge coupled device as claimed in Claim 5, characterized in that the distance between the edges of the openings in the silicon nitride layer and the edges of the windows is chosen to be equal to or greater than 1.0 μm.

7. A charge coupled device as claimed in Claim 5 or 6, characterized in that mutually adjoining charge transport channels in the semiconductor body are separated from one another substantially only by a channel bounding region, the openings in the silicon nitride layer being situated above the channel bounding regions.

8. A charge coupled device as claimed in Claim 3 or 4, characterized in that at least a number of the openings in the silicon nitride layer is provided between the surface

of the semiconductor body and electrodes which extend over the openings.

9. A charge coupled device as claimed in Claim 8, characterized in that the surface is covered by portions of the silicon nitride layer at the areas of the radiation-transmitting windows.

10. A charge coupled device as claimed in Claim 8 or 9, characterized in that the electrodes are formed in two or more silicon layers which were provided one after the other and are electrically insulated from one another, electrodes formed in a first silicon layer being insulated from the surface of the semiconductor body by a dual layer of silicon oxide and silicon nitride, while openings are present in the silicon nitride layer below electrodes which are formed in a common second silicon layer.

11. A charge coupled device as claimed in Claim 10, characterized in that openings in the silicon nitride layer have edges which lie at a distance equal to or greater than 1.0 μm from the edges of the electrodes provided above the openings.

12. A charge coupled device as claimed in Claim 8 or 9, characterized in that the electrodes are formed in two or more silicon layers which were provided one after the other and which are electrically insulated from one another, the openings in the silicon nitride layer being formed below the electrodes made from the silicon layer which was provided as the first silicon layer.

13. A charge coupled device as claimed in Claim 8 or 9, characterized in that the electrodes are formed from two or more layers of silicon, electrodes formed from a first silicon layer being separated from the surface by a first layer of silicon nitride provided with said openings, and electrodes formed from a second layer of silicon being insulated from the electrodes of the first layer of silicon by a second silicon nitride layer which is also provided with openings.

14. A method of manufacturing a charge coupled device as claimed in any one of the preceding Claims, characterized in that the openings in the silicon nitride layer are defined by means of an etching mask which was formed by photolithography and which is provided with openings through which the silicon nitride layer is subjected to an etching treatment.

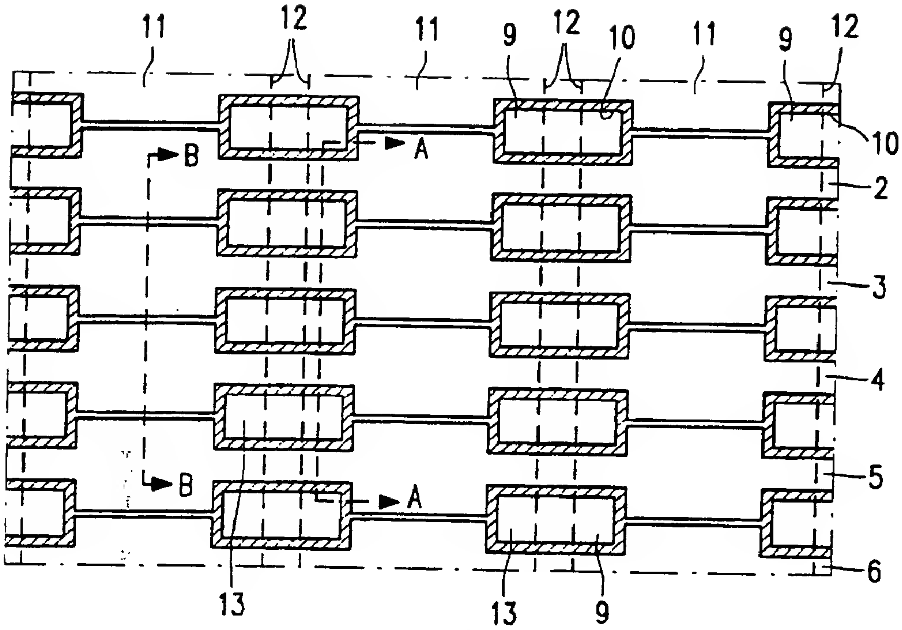

FIG. 1

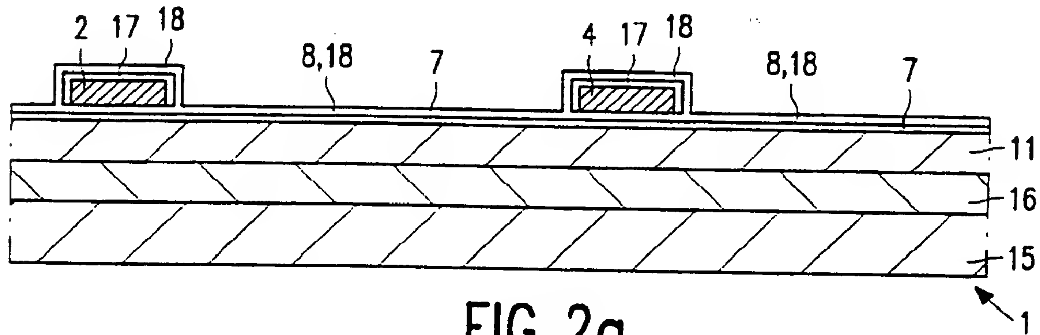

FIG. 2a

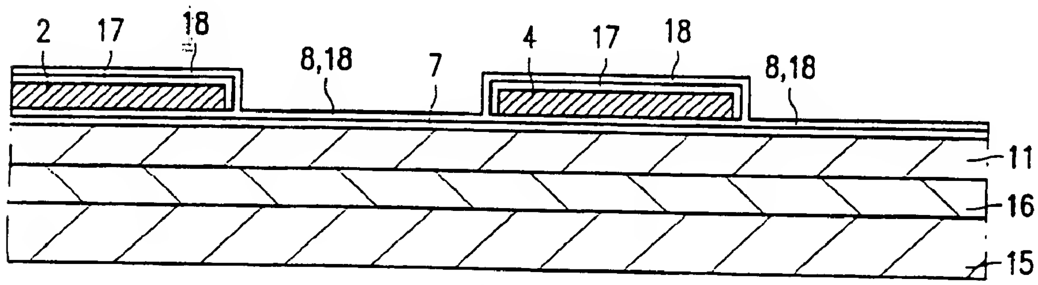

FIG. 2b

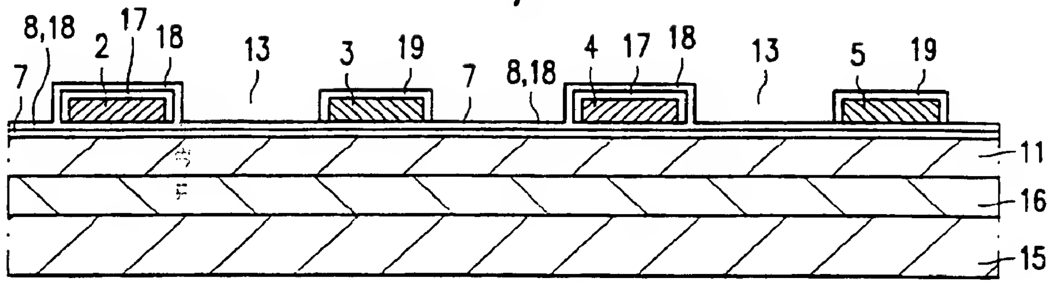

FIG. 3a

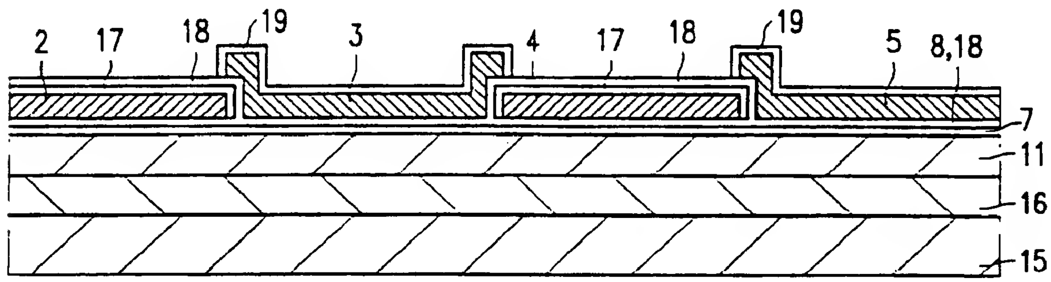

FIG. 3b

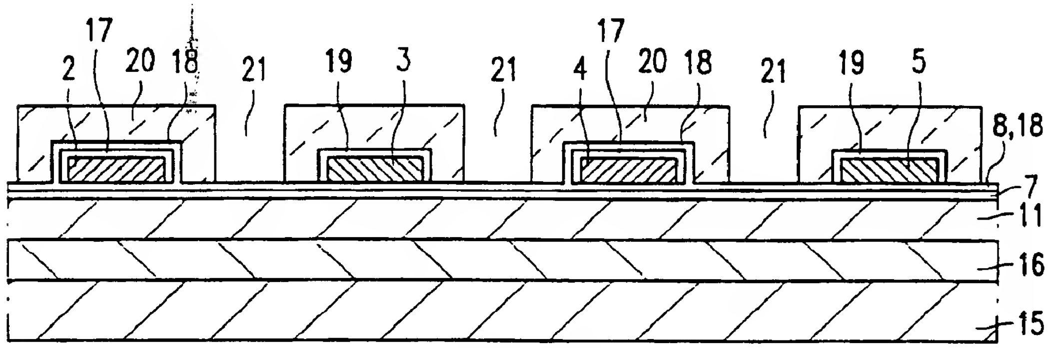

FIG. 4a

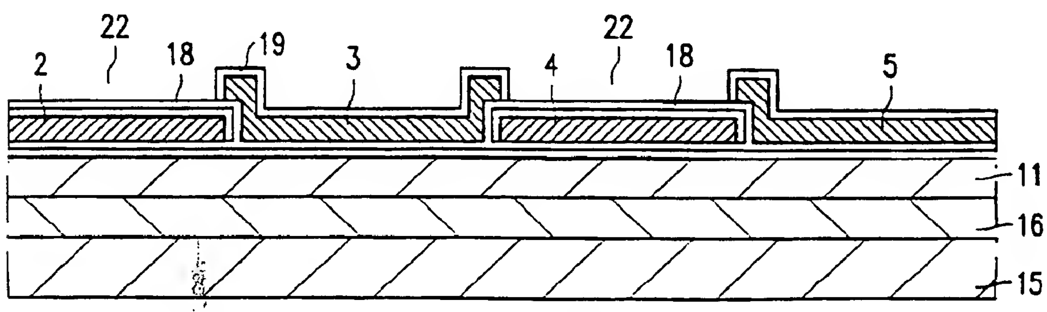

FIG. 4b

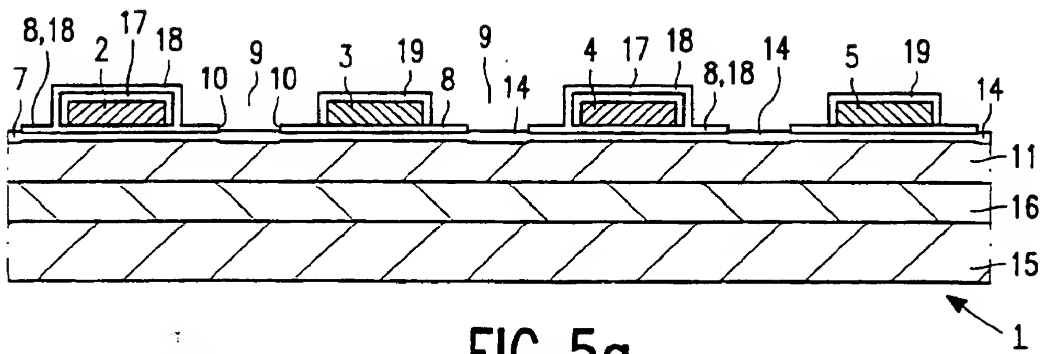

FIG. 5a

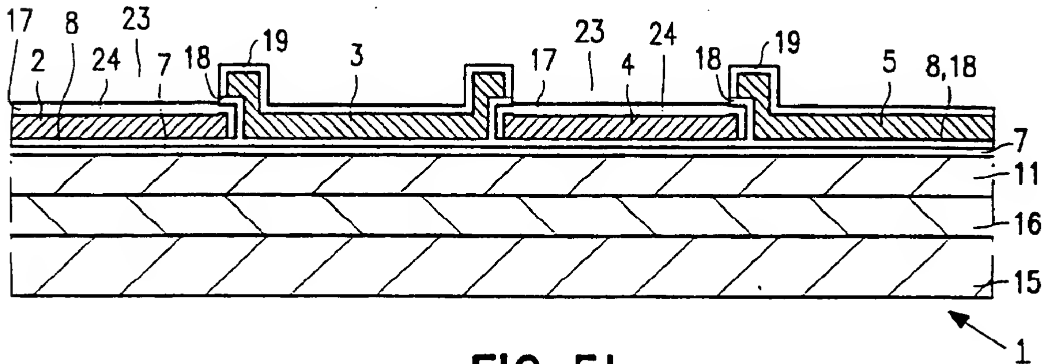

FIG. 5b

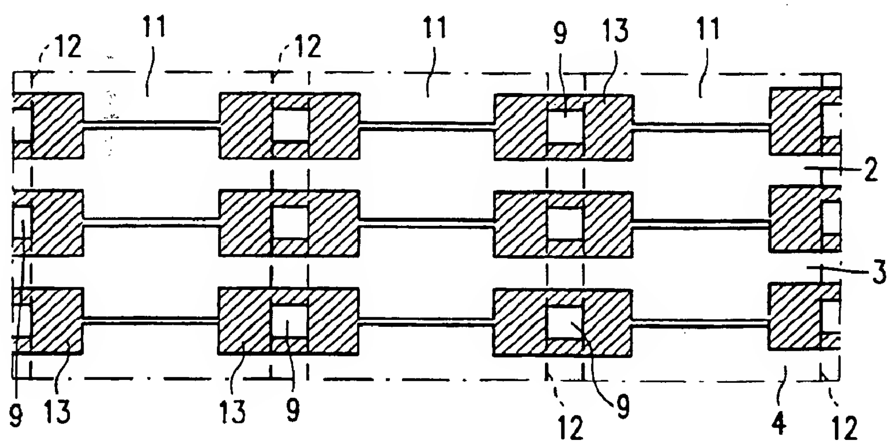

FIG. 6

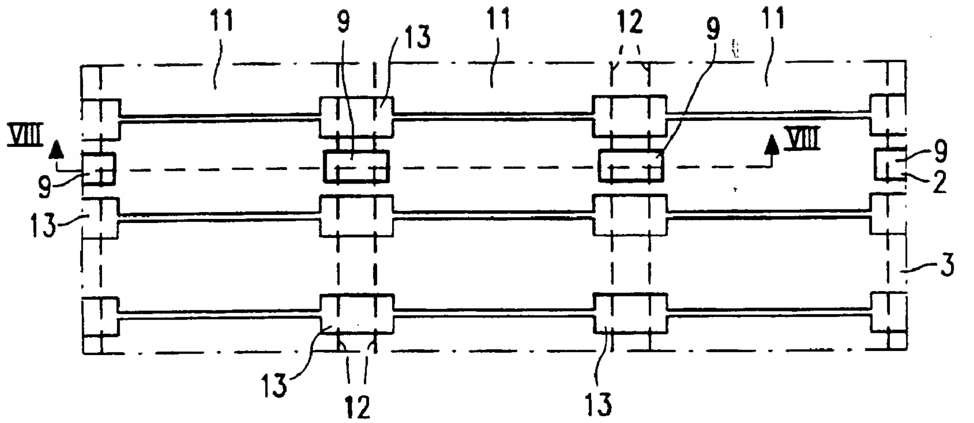
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FIG. 7

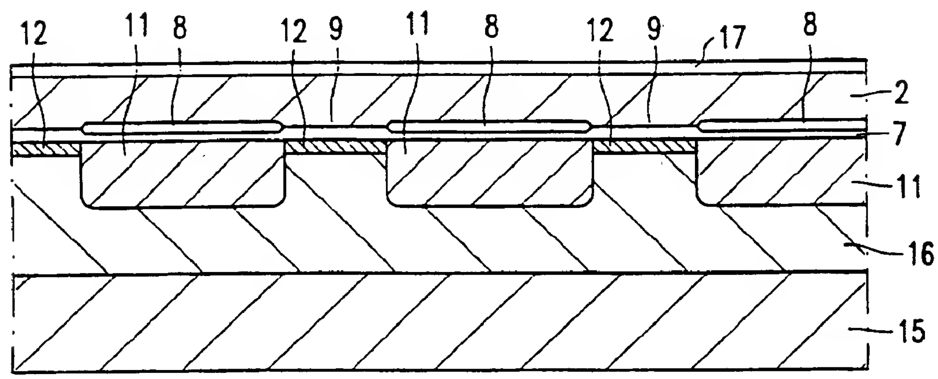
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FIG. 8

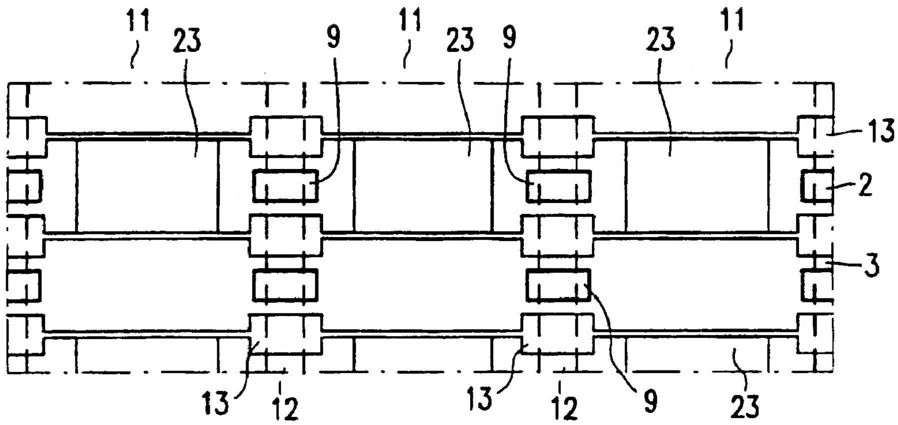

FIG. 9

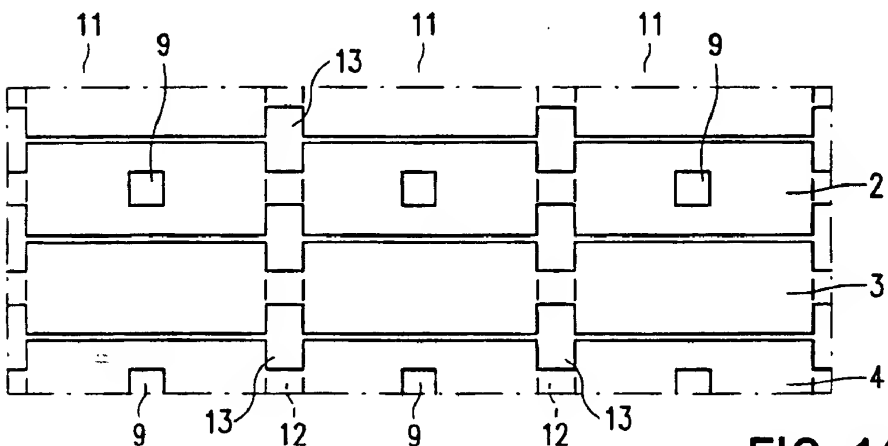

FIG. 10

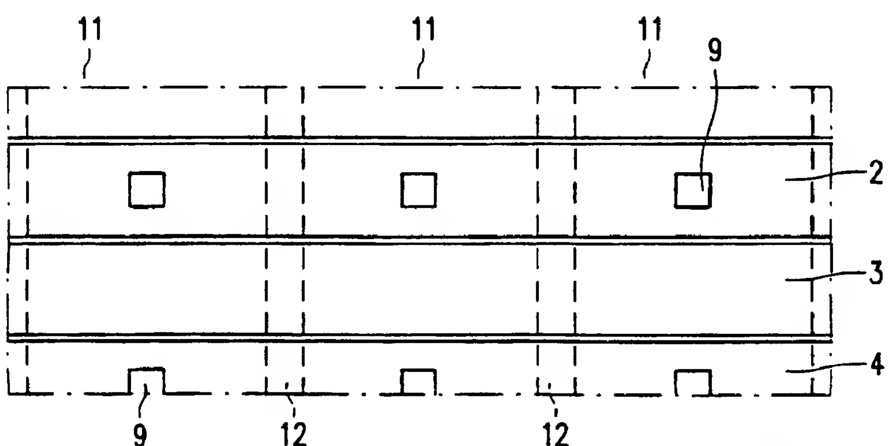

FIG. 11

INTERNATIONAL SEARCH REPORT

International application No.
PCT/IB 97/00890

A. CLASSIFICATION OF SUBJECT MATTER

IPC6: H01L 29/768, H01L 29/207, H01L 21/22, H01L 21/339

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC6: H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

SE,DK,FI,NO classes as above

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

DIALOG: 350,351

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5495116 A (HIROMASA FUNAKOSHI ET AL), 27 February 1996 (27.02.96), column 9, line 8 - line 36, figure 5 --	1,14
A	US 5065222 A (KAZUTOSHI ISHII), 12 November 1991 (12.11.91), column 3, line 25 - column 4, line 31, figure 6 --	1,14
A	US 4447272 A (NELSON S. SAKS), 8 May 1984 (08.05.84), column 2, line 63 - column 4, line 26 --	1,14

[X] Further documents are listed in the continuation of Box C. [X] See patent family annex.

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"A" document defining the general state of the art which is not considered to be of particular relevance

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance: the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance: the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
28 January 1998	29.01.1998
Name and mailing address of the ISA/ Swedish Patent Office Box 5055, S-102 42 STOCKHOLM Facsimile No. +46 8 666 02 86	Authorized officer Pär Moritz Telephone No. +46 8 782 25 00

INTERNATIONAL SEARCH REPORT

International application No.
PCT/IB 97/00890

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 4077112 A (MATTHIAS JOHANNES JOSEPH THEUNISSEN ET AL), 7 March 1978 (07.03.78), see the whole document -- --------	1-14

INTERNATIONAL SEARCH REPORT
Information on patent family members

07/01/98

International application No.
PCT/IB 97/00890

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		JP 1125940 A	18/05/89
US 4447272 A	08/05/84	NONE	
US 4077112 A	07/03/78	AU 497138 B	30/11/78
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		DE 2541651 A,C	08/04/76
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		GB 1524685 A	13/09/78
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		SE 7510593 A	25/03/76